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=> dis his

     (FILE 'HOME' ENTERED AT 13:02:37 ON 02 MAY 2002)

     FILE 'USPATFULL' ENTERED AT 13:02:47 ON 02 MAY 2002
L1   (     22831)S CACHE
L2   (   1556554)S WAY#
L3   (    489931)S LOCK?
L4             9 S CACHE (2A) WAY# (2A) LOCK? STEP
L5          2085 S LRU
L6          2557 S LEAST (W) RECENT? (W) USE?
L7          2960 S L5 OR L6
L8             3 S L7 AND L4

=> dis 1- pn,ti,ab
YOU HAVE REQUESTED DATA FROM 3 ANSWERS - CONTINUE? Y/(N):y

L8   ANSWER 1 OF 3  USPATFULL

PI     US 2001049771      A1   20011206
TI     DYNAMIC REPLACEMENT TECHNIQUE IN A SHARED CACHE
AB     A dynamically configurable replacement technique in a
unified or shared
       cache reduces domination by a particular functional unit
or an
       application such as unified instruction/data caching by
limiting the
       eviction ability to selected cache regions based on over
utilization of
       the cache by a particular functional unit or application.
A specific
       application includes a highly integrated multimedia
processor employing
       a tightly coupled shared cache between central processing
and graphics
       units wherein the eviction ability of the graphics unit is
limited to
       selected cache regions when the graphics unit over
utilizes the cache.
       Dynamic configurability can take the form of a
programmable register
       that enables either one of a plurality of replacement
modes based on
       captured statistics such as measurement of cache misses by
a particular
       functional unit or application.

L8   ANSWER 2 OF 3  USPATFULL

PI     US 5913224                 19990615
TI     Programmable cache including a non-lockable data way and a
lockable data
       way configured to lock real-time data
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AB A computer system is disclosed which provides for execution of real-time code from cache memory. A cache management unit provides the real-time code to the cache memory from system memory upon a initiation of a read operation by a processor. Once in cache memory, the processor executes the real-time code from cache memory instead of system memory. The cache management unit detects read hits to cache each time the processor requests an instruction of code that is stored in the cache memory. Lock bits associated with each line of cache lock the contents of the line preventing the line from being overwritten under normal cache operation in which the least most recently used cached data is replaced by presently accessed data. Alternatively, one of a plurality of cache data ways may be dedicated to storing real-time code. Real-time code stored in the dedicated data way is not replaceable and thus is locked.

L8 ANSWER 3 OF 3 USPATFULL

PI US 5493667 19960220
TI Apparatus and method for an instruction cache locking scheme
AB An instruction locking apparatus and method for a cache memory allowing execution time predictability and high speed performance. The present invention implements a cache locking scheme in a two set associative instruction cache that utilizes a specially designed Least Recently Used (LRU) unit to effectively lock a first portion of the instruction cache to allow high speed and predictable execution time for time critical program code sections residing in the first portion while leaving another portion of the instruction cache free to operate as an instruction cache for other, non-critical, code sections. The present invention provides the above features in a system that is virtually transparent to the program code and does not require a variety of

complex or specialized instructions or address coding methods. The present invention is flexible in that the two set associative instruction cache is transformed into what may be thought of as a static RAM in cache, and in addition, a direct map cache unit. Several different time critical code sections may be loaded and locked into the cache at different times.

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